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A Hybrid Cartesian Loop and Envelope Modulated PA Linear Transmitter Architecture.

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Abstract—A high efficiency and linearity PA solution is presented based on hybrid linearisation schemes that employ complementary techniques to overcome the weakness (or constraints) of either method on its own. In particular, the high linearity of Cartesian loop is combined with the high efficiency of Envelope Elimination and Restoration (EER). The results of a prototype hybrid linearised PA built using digital generation of the phase and amplitude signals for the EER amplifier, and utilizing a digital Cartesian feedback loop are presented. Limitations of the amplitude modulator on system performance are demonstrated using PWM and delta-modulated switching amplifiers.

Keywords—Cartesian Loop; EER; Linearization; Hybrid

I. INTRODUCTION

Linearisation of power amplifiers to meet spectral emission standards has been extensively researched and many techniques have been proposed e.g. predistortion, Cartesian loop, Envelope Elimination and Restoration (EER), polar loop, LINC, and CALLUM[1]. The techniques have allowed very high degrees of linearity, or traded wider bandwidth for moderate returns of linearity. The different techniques also have various efficiency trade-offs. In order to meet the linearity specification of current standards employing linear-modulation (e.g. varying RF envelope) linearisation methods in common usage today usually have low efficiencies. Most schemes trade efficiency for linearity. The linearisation scheme can only apply a certain amount of correction after which the power amplifier (PA) must provide the remainder, thus if high linearity is required, the PA must be more linear at the expense of power efficiency. In this context the extra linearity is obtained by operating the PA 'backed off' so that its output power is well below its peak power rating.

The market drivers for lightweight handheld terminals and long talk-time are heavily related to the technical metric of transmitter power efficiency. Cellular users currently enjoy good talk-time through the use of constant envelope modulation schemes. The next generation of cellular technology such as GSM-EDGE and UMTS use non-constant envelope modulation, as does current standards such as TETRA, and thus they must either use power efficient linearised PAs or accept much smaller lengths of talk-time. The higher data rates offered by these new technologies will be utilized by additional accessories and applications. These

accessories and applications if built into the radio will require extra power, and thus further erode the talk-time available. Future power sources such as micro-fuel-cells offer the elixir of very long talk-times[2]. Even so, the transmitter efficiency will still remain a dominating factor in the length of talk-time[3].

The focus of PA linearisation is now tending towards increased efficiency over the methods developed to date. Hybrid methods employ complementary techniques that overcome the weakness (or constraints) of any one method on its own. By removing constraints the hybrid architecture is more flexible and can cover more standards thus making it suitable for a software radio. Hybrid architectures can improve the bandwidth, linearity and efficiency above that capable of any one scheme alone.

This paper gives a brief discussion on the Cartesian loop and Envelope Elimination and Restoration (EER) transmitters (Section II & III). Then it introduces (in section IV) a hybrid architecture formed from a Cartesian loop and an Envelope Elimination and Restoration (EER) transmitter. The terminology 'EER transmitter' is not applicable in the hybrid, as the envelope is formed from the baseband signal and thus no elimination is encountered. Thus, the EER portion of the hybrid is simply termed envelope modulation instead.

In the hardware prototype hybrid built, it was found that the bandwidth of the amplitude modulator limited the stability of the Cartesian loop. This paper demonstrates the amplitude modulator bandwidth limitation using a PWM based amplitude modulator and a delta modulator based amplifier. Further, it is shown (in section V) that the later suffers from hard non-linearities due to slope-overload, and that the former is a more benign choice to include in a feedback loop. Finally it is noted that high speed power-switching[4], or interleaving methods[5] are necessary in order to meet the bandwidth requirements of today's standards.

II. EER TECHNIQUE

Figure 1 shows a conventional EER transmitter. The RF signal $s(t)$ is separated into its envelope and phase components (i.e. polar co-ordinates). The PA amplifies the constant-envelope phase signal, and the envelope signal modulates the voltage supply to the PA.

The detection of the envelope and phase signals is a non-linear process and therefore the bandwidth of these components

is much larger than the RF signals bandwidth, this phenomena is termed 'bandwidth expansion'. For example, consider the envelope of a two-tone signal (with 1 kHz spacing), which is simply a rectified 1 kHz sinewave. The Fourier components of the envelope extend to infinity, i.e. the envelope bandwidth is infinite. Similarly the phase signal of a two-tone signal is a square wave with period of 500 Hz, and therefore also has an infinite bandwidth. Generally the envelope and phase bandwidth is limited to a finite bandwidth that results in acceptable distortion levels in the recombined signal

The PA amplifies the constant-envelope phase signal, and the envelope signal modulates the voltage supply to the PA. By envelope modulating the power amplifier, which is a class C stage, the efficiency can be greatly enhanced.

The EER transmitter whilst simple, achieves only modest amounts of correction primarily limited by carrier feedthrough in the PAs active device[6].

The addition of envelope feedback is popular and some implementations of this have achieved intermodulation distortion (IMD) of -30 to -50 dBc (for 1W to 20W) and efficiencies of up to 50% [7,8,9]. Envelope feedback corrects for amplitude errors only, however by using Cartesian feedback, the amplitude and phase distortion at the PA output can be corrected. The use of phase correction is necessary to compensate for carrier feedthrough in the PA active device.

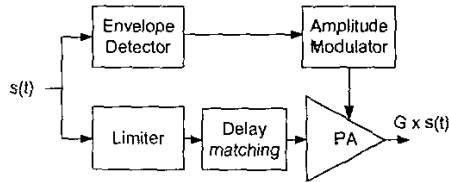


Figure 1. Envelope Elimination & Restoration (EER)

III. CARTESIAN FEEDBACK

Cartesian feedback is a negative feedback technique that demodulates the RF signal and uses the quadrature baseband signals as the feedback signal. In this way the feedback loop is less sensitive to delays than if the feedback occurred at RF. Because of this reduced sensitivity more loop gain can be tolerated, resulting in greater suppression of non-linearities.

Linearity, stability and bandwidth are traded off in the design flow[10]. RF group delay (and baseband delays) τ , reduce the loop stability and the compensation filter (with bandwidth ω_L) is designed to stabilise the loop whilst achieving as wider loop bandwidth as possible. Generally the compensation filter is not a straightforward low pass filter but includes lead/lag networks. The use of wide bandwidth gain stages is important to reduce the effects of additional poles that can decrease the phase margin. The stability of the Cartesian loop for a simple 1st order loop filter is given by,

$$PM_{\text{Radians}} = \pi - \sqrt{\omega_L^2 (\alpha^2 \beta^2 - 1)} \tau - \tan^{-1} \left(\sqrt{\alpha^2 \beta^2 - 1} \right) \quad (1)$$

where α is the forward path gain, and β the feedback path gain. For high open loop gain $\alpha\beta$, the phase margin can be approximated as,

$$K = \omega_L \alpha \beta \tau \quad (2)$$

where $K = \pi/2 - PM_{\text{Radians}}$, and PM_{Radians} is the phase margin. The open-loop-gain is chosen according to the IMD suppression needed i.e. for $\alpha\beta \gg 1$, the distortion suppression is,

$$G_D \approx \frac{1}{\alpha \beta} \quad (3)$$

The actual suppression the Cartesian loop is required to give is determined by the uncorrected linearity of the PA. Its linearity can be increased by operating it backed off, hence reducing the suppression needed and therefore the open-loop gain needed. However to achieve the required output power implies a transmitter with higher peak power, which in turn implies low efficiencies. Thus a design trade-off between efficiency, linearity and stability of components exists, which makes high performance Cartesian loops difficult to design to also achieve high efficiencies.

The phase shifter is needed to counter for RF phase delays[11]. This must be set uniquely for every channel, and generally requires a training sequence to optimize the setting. Another source of error in Cartesian loop is due to DC offsets, if uncorrected these cause carrier feed through [12] requiring additional circuitry to cancel out the DC offsets. The DC offsets and phase shifter must be calibrated, usually a calibration period is used where training signals are used to adjust the phase shifter and DC offset circuitry. If the monitoring of the training signals is via open loop techniques then switches are required prior to the feedback summing point.

A new method of implementing Cartesian loop utilizes an all-digital baseband section [13]. The digital baseband allows the phase shifter to be implemented in the digital section as a matrix rotation of the I and Q signals, as opposed to analog Cartesian loops, which require a bulky phase shifter operating on the LO to either the quadrature modulator or demodulator. Further advantages arise from increased integration and ease of calibration as all calibration factors can be applied digitally. The new method is particularly suited to implementing hybrid architectures

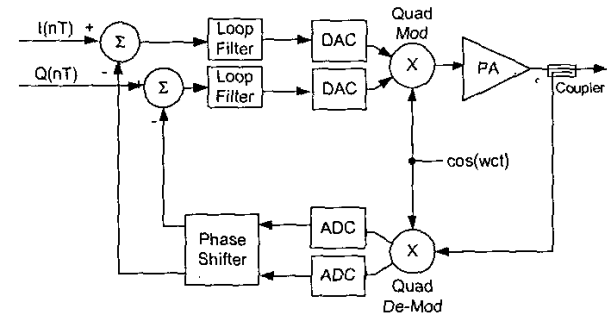


Figure 2. Envelope Elimination & Restoration (EER)

IV. HYBRID METHOD

For modern applications The EER transmitter has the limiter and envelope detector replaced with digital processes that generate the envelope and phase signals directly from the baseband signals.

The use of Cartesian feedback replaces or aids envelope feedback, as well as reducing time delay mismatches and phase distortion. As the envelope and phase generation processes are now inside the Cartesian loop, their specifications may be relaxed. Conversely, as the envelope modulated PA gives better linearity than a class AB power amplifier e.g. -40 to -50 dBc versus -25 to -35 dBc, then the Cartesian loop does not have to add as much linearity. This should allow the loop gain of the Cartesian loop to be reduced, increasing its stability or bandwidth.

Figure 3 shows a block diagram of the prototype hybrid architecture. The digital logic was implemented using a Xilinx XCV200, the feedback ADCs was an AD9201, and the DAC an AD9750. The sampling rate was 10MHz. And the RF operating frequency was 400 MHz.

The efficiency of the hybrid was deliberately lower than is possible, as the hardware was designed with flexibility in mind, not low power design. The PA efficiency was $\approx 60\%$, and the SMPS in the amplitude modulator achieved an efficiency of 87%. The total power consumed by the transmitter to produce 1 Watt of RF power is given in Table 1, along with probable power consumption should state-of-the-art integration and design processes be used.

Table 1. Efficiencies of Hybrid Architecture

	Actual Prototype	Probable
Digital logic (plus ADCs and DACs)	800 mW	50 – 100 mW
Amplitude Modulator	150 mW	50 – 100 mW
Power Amplifier	1540 mW	1450 – 1500 mW
Quad. demod	150 mW	50 – 100 mW
Quad. mod. and RF driver	650 mW	300 – 350 mW
Total	3290 mW	1900 – 2150 mW.

From Table 1 it is seen that the prototype transmitter achieves only 30.5% efficiency, but the probable efficiency of an integrated and more sophisticated design could easily achieve 45-50%.

It is worth noting that if the PA was replaced by a linear line-up and biased to achieve the same linearity it would have an efficiency of perhaps 40%, and the total transmitter efficiency would be $\approx 24\%$. This serves to illustrate that the hybrid prototype does give a substantial gain in efficiency in its current configuration, especially as efficiency gains at low efficiencies translate into higher gains in battery life or talk time[3].

The Hybrid method was implemented using two different amplitude modulators. PWM offers a simple architecture but its performance relies on an accurately generated triangle wave.

Delta-modulation also has a simple architecture, and offers the advantage of wider bandwidth (for the same switching rate) than PWM[14]. Due to the predictive nature of delta-modulation (i.e. the integrator in the feedback of a delta-modulator, is a prediction filter), the output of the prediction filter is in phase with the input to the delta-modulator. Thus, unlike PWM, the loop filter in the delta modulator does not cause a large time-mismatch between the phase and envelope paths.

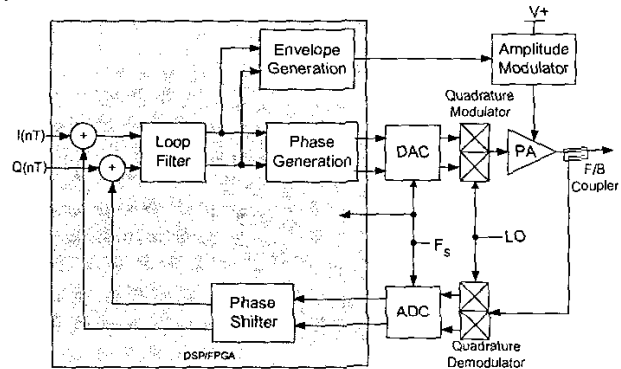


Figure 3. Hybrid Cartesian Loop and Envelope Restoration Linearisation.

V. AMPLITUDE MODULATOR

A. Delta Modulation.

Figure 4 shows an amplitude modulator setup in a delta-modulator configuration. The familiar digital output of the delta-modulator is the output of the quantiser block. The output used to modulate the PA is the output of the prediction filter, i.e. the LC filter. Note, it is possible to implement the comparator digitally removing the DAC and analog comparator, however this requires an additional ADC, which for a low power version, results in increased delay and therefore quantisation (granular) noise in the delta-modulator output.

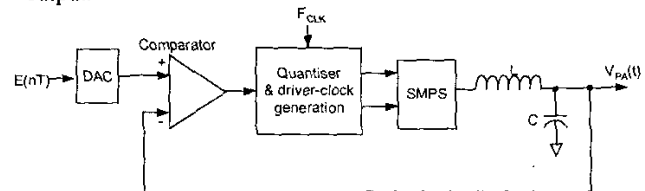


Figure 4. Amplitude Modulator utilizing Delta Modulation

The bandwidth of a delta-modulator for this work is defined as the point where the slope overload distortion begins to increase for a full-scale input. At this point if the input amplitude is reduced the slope overload distortion reduces. Hence as long as the amplitude of the envelope is reducing faster than the rate of filter roll-off no increase in slope-overload distortion will be incurred. This allows the bandwidth of the delta-modulator filter to be set much lower than the envelope signals bandwidth, e.g. instead of 5 times the RF

bandwidth, it was found that equal to the RF bandwidth was suitable.

Figure 5 shows the performance of the hybrid with the delta-modulator filter set to 26 kHz and damping factor of 0.62, the clock rate was 3.33 MHz. For a $\pi/4$ DQPSK signal (18 kbaud, $\alpha = 0.35$). For maximum loop gain, the correction achieved in the 1st ACP was -53 dBc, 15 dB better than the open loop case (i.e. EER amplifier only).

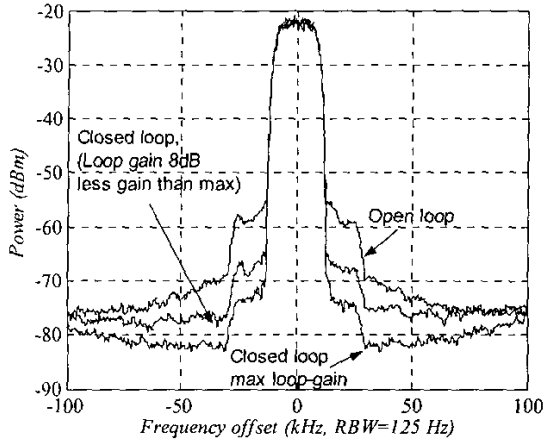


Figure 5. Results of hybrid transmitter with delta-modulator

Reducing the damping factor to 0.26 and bandwidth to 21 kHz reduces the extra correction from the feedback to 3.5 dB, a drop of 11.5 dB over the previous filter bandwidth. The reduction in performance is due to increased slope overload in the delta-modulator caused by the action of the Cartesian feedback.

In regions of high envelope slew rate, the output of the delta modulator does not slew as fast, this is particularly true at envelope minima which occur close to zero amplitude. The PA will not faithfully reproduce these minima, due to carrier feedthrough not allowing it to fully turn-off. At these instances the action of the feedback is to predistort the signal into the amplitude modulator to compensate for the distortion at the PA output. This increases the slew rate into the delta-modulator, and if its bandwidth is not large enough, it will have increased slope overload distortion. This in turn leads to a local instability in the feedback loop, and can only be avoided by reducing the loop gain, and therefore the correction obtainable (see Figure 6).

Increasing the bandwidth of the delta-modulator is detrimental to the wide-band noise of the amplitude modulator. In Figure 5 the wideband noise can be seen to be increasing at higher offsets from the channel center frequency. Hence Delta-modulation has a trade-off between linearity and noise performance exists.

B. PWM

A disadvantage of PWM is the linearity of the triangle generator. By implementing the triangle generator digitally, see Figure 7) the limitation to linearity is the sampling rate F_s to

clock rate F_c , as well as the resolution of the triangle wave and signal, additionally no DACs or ADCs are needed.

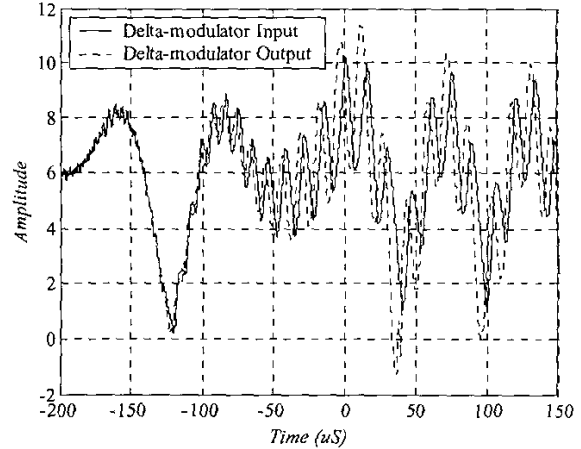


Figure 6. Instability due to the envelope being driven negative

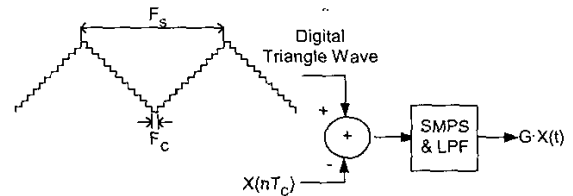


Figure 7. Digital PWM

The complexity of Figure 7 is simpler than the delta-modulator, however the bandwidth is less for the same sampling rate, F_s . To achieve a sampling rate of 1 MSPS using an eight bit envelope requires a 512 MHz clock. Hence it is difficult to achieve a high sampling rate for PWM generated this way.

The implementation of PWM using Figure 7 was clocked at $F_c = 200$ MHz. The triangle wave resolution was seven bits giving a sampling rate of $F_s = 781.3$ kHz. The first ACPR was -30, -37.8 & -40 dBc for the 6, 7 & 8 bit implementations respectively. The use of the above digital technique is crude, and requires at least an eight-bit resolution to achieve performance comparable with the delta-modulator. To raise the PWM sampling rate further, either analog PWM is needed or a more sophisticated version of Figure 7 that allows higher sampling rates is needed[15].

The PWM filter used a LC filter (as for the delta-modulator). Initially the PWM filter was trialed as the Cartesian-loop-filter, i.e. the Cartesian-loop filter was removed and the PWM filter bandwidth set to 25 kHz. This was unsuccessful as the second order response of the filter reduces the phase-margin to quickly, and no useful reduction in distortion can be obtained before the system goes unstable. Additionally the time mismatch is $> 3 \mu s$ and any attempt to introduce a delay of this magnitude into the phase path will have an immense impact on the stability of the loop.

The filter bandwidth was extended to 200 kHz and Figure 8 shows the open loop and closed loop results for this filter. The open loop ACP is -37.8 dBc, -47.6 dBc, & -54.1 dBc in the 1st 2nd & 3rd adjacent channels respectively. Attempts to implement time-delays in the phase path made no improvement in the ACP, and the limit on linearity is dominated by the PWM implementation and driver feed through.

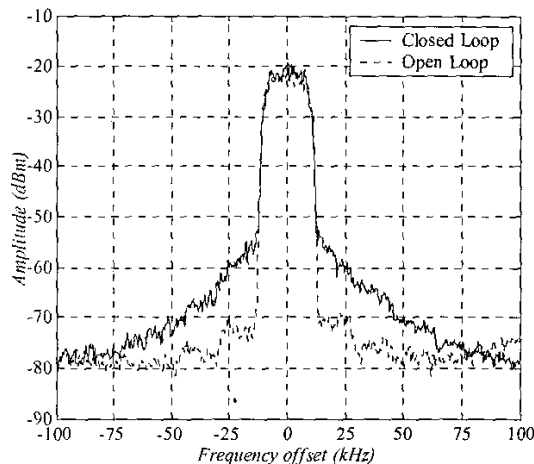


Figure 8. Results of hybrid transmitter with PWM

The closed loop response shows a significant improvement in the ACP, with 11.8 dB, 8.2 dB, & 1.1 dB of correction being obtained in the 1st 2nd & 3rd adjacent channels respectively. The ACP was -49.8 dBc, -55.8 dBc, & -55.2 dBc in the 1st 2nd & 3rd adjacent channels respectively.

The limit on further correction is due to the Cartesian-loop stability, which is dominated by the filter bandwidth of the PWM filter. No non-linear dynamics are present, unlike the delta-modulator case. To further increase the linearity of the hybrid with the PWM filter requires the PWM filter to have a greater bandwidth, and therefore a greater sampling rate.

VI. CONCLUSIONS

This paper has shown a method of achieving high linearity and high efficiency through the hybrid method of Cartesian loop and EER linearisation. The EER or envelope modulation provides high efficiency and modest linearity of -40 dBc, whilst the Cartesian Loop has been demonstrated giving an additional 13 dB of linearity, for a total linearity of -53 dBc.

PWM has been shown to be a more benign choice for the envelope amplifier over delta-modulation. The delta-modulator caused instabilities at high signal slew rates, increasing the delta-modulators bandwidth to overcome the slew rate limitation leads to increased wideband noise. For PWM the limit of linearity is the bandwidth of the PWM filter, The effects of which are predictable from linear stability analysis[6]

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